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FPGA Based Implementation Of Baseband OFDM Transceiver Using VHDL

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***Abstract*— Orthogonal Frequency Division Multiplexing (OFDM) is a multicarrier communication system. It is widely used because of its immunity to frequency selective fading channels. In this paper, the design and an implementation of OFDM transceiver on FPGA is presented. The system is designed using VHDL, synthesized using high level synthesis tool and targeted on Xilinx Spartan 3e device. Presented design is simulated on ISE simulator and the results are presented. Resources utilization for transmitter and receiver is given in this paper. The design utilizes the Intellectual Property (IP) cores provided by Xilinx for floating point multiplication, addition subtraction and division. DIT radix-2 butterfly approach is used to calculate IFFT and FFT.**

Keywords-FPGA, FFT, IFFT, DIT, ISE, VHDL.

I. INTRODUCTION

The modern digital mobile communication systems are increasingly using baseband OFDM for multi-carrier transceiver. Idea behind the high spectral efficiency of OFDM is elimination of guard bands and use of the overlapping but orthogonal subcarriers. High rate data stream is divided into a number of low rate data streams that are transmitted over a number of multiplexed orthogonal subcarriers [1]. The low rate data streams allow adding sufficient guard time between two symbols which was very small in high rate data stream. This helps in enabling the system to perform well in dispersive channel which causes the symbols to spread in time and interfere with each other called as inter symbol interference (ISI).

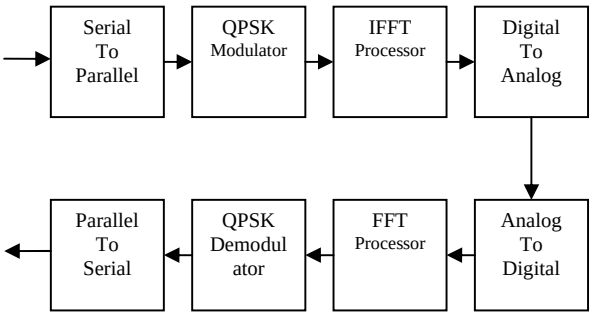

Fig 1 Block diagram of basic baseband OFDM system

OFDM can be viewed as either a modulation or multiplexing technique, and its hierarchy lies in the physical and medium access layer. A basic OFDM transceiver consists of a QAM or PSK modulator/demodulator, a serial to parallel/parallel to serial converter, and an IFFT/FFT module [1]. The block diagram of basic OFDM system is shown in Fig 1. The transmitter consists of a input bit stream, serial to parallel converter, constellation mapping, IFFT, DAC. The receiver consists of ADC, FFT, parallel to serial converter, demodulation, and output bit stream.

This paper is organized as follows. Section II presents the design flow to implement an OFDM transceiver from system design to circuitry realization on FPGA. The implementation aspects of the transmitter and receiver are demonstrated in section 3 and 4. The results are discussed in section 5 and finally the conclusion is given in section 6.

II. DESIGN FLOW

Initially transmitter and receiver is implemented independently and tested on kit, and then both the subsystems were merged to form one system. The system is designed for two sets of subcarriers one is using 4 subcarriers and the other using 8 subcarriers. Design flow for both the system is same. It is explained as follows.

The design of system starts with the understanding of the block diagram. It gives the idea about operations needed to be performed with help of FPGA. Then the algorithm is developed for the sequential and concurrent operations. To make the design more parallel the operations are broken in to processes and independently written in VHDL. Some blocks contain floating point complex operations, for that Intellectual Property (IP) cores provided by Xilinx are used. IP cores are used for all types of floating operations.

The system is designed completely on Xilinx Project Navigator using VHDL coding as design entry method. Then the system is simulated on ISE simulator for timing analysis. Finally the design is synthesized on FPGA Spartan 3e device using high level synthesis tool.

III. TRANSMITTER DESIGN

A. Transmitter design Flow

Input bit stream of length 16 bit is stored in the array. Serial to parallel conversion is done in independent process which simultaneously maps the parallel, grouped bits in to complex constellation for QPSK. Two different arrays are utilized to store real and imaginary parts of constellation points. Look up table is used to map grouped bits in to constellation. An algorithm is developed for IFFT calculation. Complex multiplications are involved in 8 point IFFT calculations. Twiddle factors are stored in array, which are necessarily floating point. The floating point complex multiplications are done using the algorithm. IFFT calculator is multistate process which uses different IP cores for specified operations. Two separate systems are designed using 4 subcarriers and 8 subcarriers. To have different number of subcarriers means changing the points in IFFT calculation A separate process maps the real and imaginary values in the range of DAC and transmits them through separate channels. DAC used for this purpose is LTC 2624 which is interfaced with FPGA through SPI communication. For transmitting particular OFDM symbol through DAC it must be converted in the format that is acceptable by DAC. Then this control word is transmitted serially to DAC with control signals to start the conversion.

B. Comparative analysis of transmitters

The presented system is implemented using 4 subcarriers and 8 subcarriers. The effect of increasing the number of subcarriers on computational complexity to calculate the IFFT is shown in Table I. Number of clock cycles required to perform the operation are given in Table I.

TABLE I
COMPARATIVE ANALYSIS OF TRANSMITTERS

Parameter	4 point	8 point
Number of Complex multiplications	1	5
Number of Complex additions	8	24
Number of divisions	8	16
Number of clocks for multiplications	1	95
Number of clocks for additions	2	75
Number of bits in an OFDM symbol	8	16

Table I describes the number of operations needed to be performed on a one set of data to convert it from bit stream to OFDM symbol. The comparison shows that 8 point system requires more time but it receives more number of bits per OFDM symbol.

IV. RECEIVER DESIGN

In presented system the receiver is designed on the same board. The data after the IFFT block is directly given to FFT block of receiver. The design flow of the receiver and the comparison between 4 point and 8 point receiver is presented in following sections.

A. Receiver design flow

Receiver is designed separately before connecting it to transmitter. FFT is calculated using an algorithm developed for transmitter. DIT radix-2 butterfly is used to calculate FFT and IFFT. The receiver is designed on Xilinx Project Navigator using VHDL coding. Similar to transmitter, receiver also uses the IP cores for floating point complex multiplication, additions and subtractions. Receiver operations are broken in to different processes and merged to have complete system. After FFT operation, demodulation is done for demodulation look up table approach is used. Once the bits are recovered from the received constellation, the reception is completed. For 4 point and 8 point transmitter separate receivers are designed and tested. Once the design code is ready it is simulated on ISE simulator for timing analysis and then synthesized on kit.

B. Comparative analysis of receivers

Receivers are different for 4 point transmitter and 8 point transmitter. This section presents the comparison of different receivers on the basis of computational complexity and time in terms of number of clock cycles required to perform the operation. The comparison is shown in Table II.

TABLE II
COMPARATIVE ANALYSIS OF RECEIVERS

Parameter	4 point	8 point
Number of Complex multiplications	1	5
Number of Complex additions	8	24
Number of divisions	8	16
Number of clocks for multiplications	1	95
Number of clocks for additions	2	75
Number of bits in an OFDM symbol	8	16

Table II describes the number of operations needed to be performed on a one set of data to convert it from bit stream to OFDM symbol. The comparison shows that 8 point system requires more time than 4 point system but it receives more number of bits per OFDM symbol.

Both the transmitters and receiver are simulated on ISE before they are synthesized on FPGA. ISE results help in understanding the timing ambiguities and in resolving the conflicts between different internal signals. Next section explains the results of simulation based on that the conclusion can be made.

V. RESULTS

The designed system on Project navigator is simulated on ISE simulator. The results are tested section wise i.e. transmitter is tested first and then receiver. Then total system is simulated. Simulation results are presented here and comments are given after each result. The resources utilized by the system are also shown in this section. Resources utilization per subsystem is given[11].

A. *Transmitter side results*

Code for transmitter is simulated on ISE simulator which gives the results as shown in Fig 2.

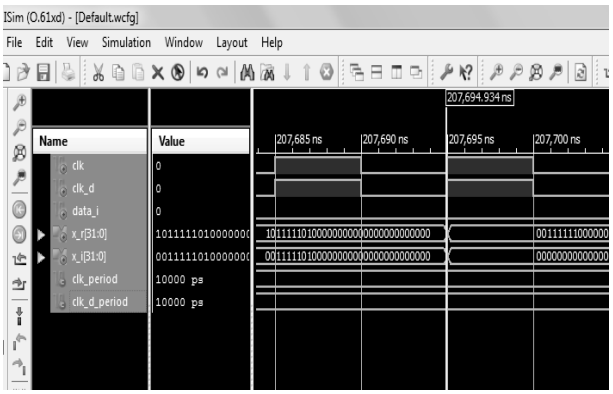

Fig 2. Data after IFFT operation, x_r and x_i represents the OFDM samples.

The above Fig 2 shows the output of simulator, x_r and x_i represents the real and imaginary arrays that hold the complex data after IFFT is done. This data is transmitted one by one at each clock through DAC. IEEE 754 standard is used to represent the floating point results. Above Fig 2 is taken from output window of simulator.

The number of clock cycles required to form the OFDM symbol can be counted from the output window. Based on timing analysis the performance of the system can be analyzed.

B. *DAC Testing*

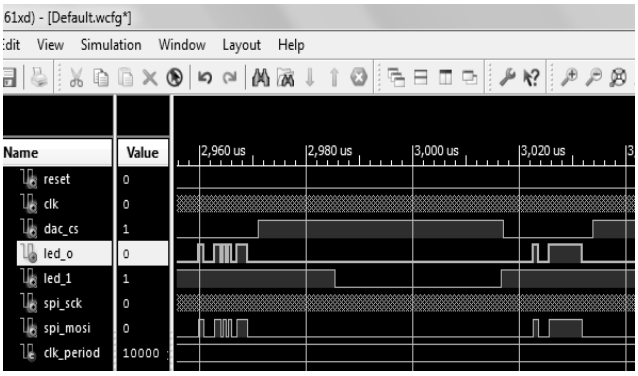

Fig 3. Serial Output from FPGA to DAC over soi_mosi pin.

Once the OFDM symbol is formed through IFFT then remaining task is to represent it in time domain, this can be done through DAC. Serial communication is used for data transfer between FPGA and DAC. The data to be transmitted serially through output pin is shown in Figure3. Synchronization between the clock, control signal and the data can be seen in the Figure 3.

C. *Receiver side results*

Receiver should ideally detect all the bits it is receiving. The result of simulation shows that receiver decodes every bit correctly. The result of simulation is shown in Figure 4.

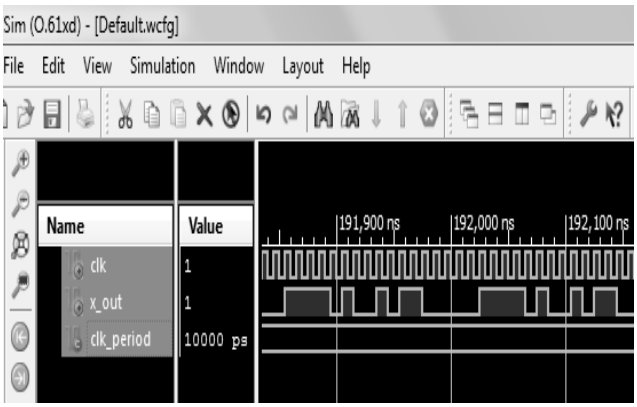

Fig 4. Output of receiverafter all operations performed on OFDM signal

Fig 4 shows the received bit stream which is exactly same as the transmitted bit stream. The received data is shown with respect to clock. Resources utilization for transmitter and receiver is shown in next section

D. *Kit tested on DSO.*

Fig 5 shows hardware connection and testing of system on DSO.

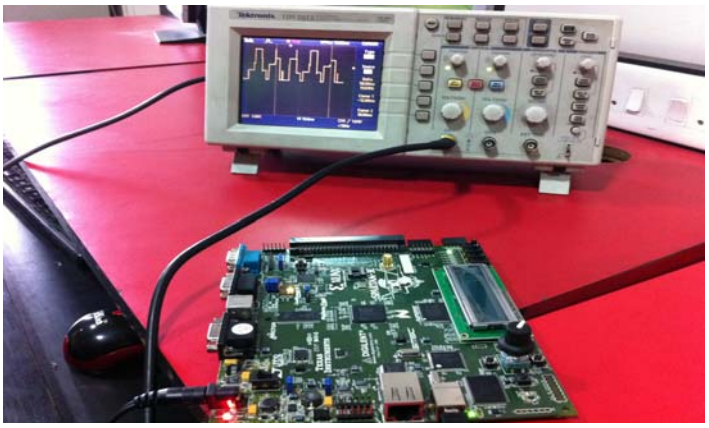

Fig 5. Output of VHDL code burnt on kit for DAC interfacing tested on DSO.

E. *Resources utilization*

1) *Transmitter side utilization*

Xilinx synthesis tool generates the device utilization summary in synthesis report after synthesis of VHDL code. Table III shows transmitter side FPGA device utilization.

TABLE III
DEVICE UTILIZATION SUMMARY FOR TRANSMITTER

Logic Utilization	used	present	Usage
Number of Slice Flip Flops	3195	9312	34%
Number of 4 input LUTs	7828	9312	84%
Number of occupied slices	4448	4656	95%
Number of slices containing related logic	4448	4448	100%
Number of slices containing unrelated logic	0	4448	0%
Total Number of 4 input LUTs	7924	9312	85%
Number of bonded IOBs	74	232	31%
Number of MULT 18X18 SIOs	4	20	2%

2) Receiver side utilization

Hardware resources utilization of Spartan 3 device is shown in Table IV.

TABLE III
DEVICE UTILIZATION SUMMARY FOR RECEIVER

Logic Utilization	used	present	Usage
Number of Slice Flip Flops	3228	9312	34%
Number of 4 input LUTs	5366	9312	57%
Number of occupied slices	4032	4656	86%
Number of slices containing related logic	4032	4032	100%
Number of slices containing unrelated logic	0	4448	0%
Total Number of 4 input LUTs	5437	9312	58%
Number of bonded IOBs	4	232	1%
Number of MULT 18X18 SIOs	4	20	2%

VI. CONCLUSION

Main aim of this paper is hardware implementation of OFDM system on Spartan 3 FPGA using VHDL language for designing the system. The system design procedure, tools and results are discussed in this paper. From the results of simulation it can be concluded that as we increase the number of subcarriers in the system, processing time required to calculate IFFT and FFT also increases. The advantage of increasing the subcarrier is the increased spectral efficiency of the system.

Results show that the system is working correctly. Device utilization of the transmitter and receiver shows that the device is utilized well bellow its capacity. Further by increasing the number of subcarriers and by making highly pipelined architecture for IFFT and FFT the system performance could be improved in terms of processing time required in transmitter and receiver.

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